## ABSTRACT OF THE DISCLOSURE

A device has a bit line pair including first and second bit lines, a sense amplifier commonly connected to the bit line pair, and first and second cells connected at intersecting 5 portions of first and second word lines and the first and second In a normal mode, the first and second word lines bit lines. are assigned separate addresses, whereas in a partial mode, the first and second word lines are assigned the same address. first and second cells complimentarily store one bit of data. In storing a data in a first cell of two cells comprised in a 10 twin cell into a second cell when set to the partial mode, the second word line is activated based on a trigger signal generated by a refresh timer during a precharge period for the bit line pair, and subsequently the precharge is completed. The first word line is then activated based on a delayed signal of the 15 trigger signal, and the sense amplifier is activated to amplify a differential voltage between the bit line pair, so that the data of the first cell is written back into the first and second cells.